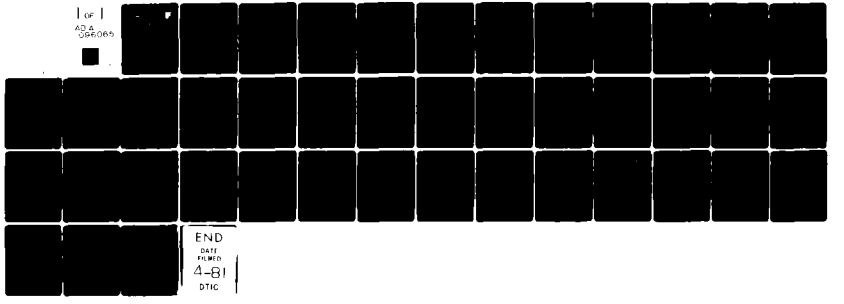
AD-A096 065 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/2
ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES. PART II. ASSES--ETC(U)
JAN 81 R A MOYERS, P PFEIFFER, F TEITZE F30602-79-C-0162
UNCLASSIFIED RADC-TR-80-401-PT-2 NL



AD A095065

LEVEL II

(12)

(18) (19)

RADC-TR-80-401, Part 2 (of two)

(9) Final Technical Report. Jun 79 - Sep 80.

(11) Jan 1981

(6)

ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES. Part II. (NH)
Assessment of a Circuit Implementation to Measure EPROM Data Storage Margins.

IBM Corporation

(10) R.A. Moyers
P. Pfeiffer
F. Teitze

(12) 42

(15) F30602-79-C-0162

(16) 2338 (17) 01

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-80-407, *Part 2 (of two) has been reviewed and is approved* for publication.

APPROVED: Allen P. Converse

ALLEN P. CONVERSE
Project Engineer

APPROVED: David C. Luke

DAVID C. LUKE, Colonel, USAF
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRA), Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-80-401, Part 2 of (two)	2. GOVT ACCESSION NO. AD-A096065	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES Assessment of a Circuit Implementation to Measure EPROM Data Storage Margins	5. TYPE OF REPORT & PERIOD COVERED Final Technical Report June 1979 - September 1980
	6. PERFORMING ORG. REPORT NUMBER N/A
7. AUTHOR(s) R. Moyers P. Pfeiffer F. Teitze	8. CONTRACT OR GRANT NUMBER(s) F30602-79-C-0162
9. PERFORMING ORGANIZATION NAME AND ADDRESS IBM Corporation Federal Systems Division Manassas VA 22110	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 23380185
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (RBRM) Griffiss AFB NY 13441	12. REPORT DATE January 1981
	13. NUMBER OF PAGES 44
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION, DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Allen P. Converse (RBRM)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

UV EPROM	Floating Gate
Memory	Threshold Voltage
Reliability	Programmed and Erased Margin
Data Retention	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes work performed from June 1979 to February 1980 to assess the utility of an EPROM threshold margin measurement concept, which minimizes the need to guarantee long term data retention in EPROM in critical military applications.

In this concept, special circuitry included on-chip allows a user to periodically measure, from normal external package pins, the programmed

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

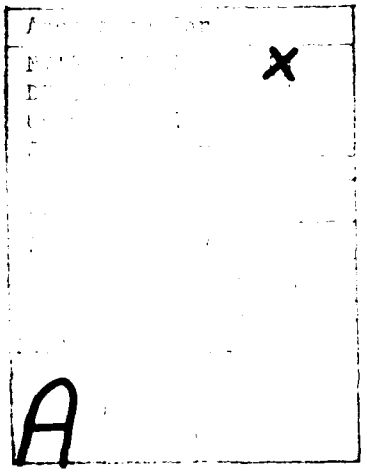
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

and erased threshold margins of every cell in the array. A device possessing this special mode in its entirety was not available. However, a single vendor did incorporate (for this and other purposes) a similar function in his 16K EPROM. While this device is useful as an evaluation tool, due to its inherent inability to measure the threshold of an erased cell, it is inadequate to rigorously validate the proposed concept.

An electrical characterization and an analysis of the test mode circuitry was performed on the vendor's EPROM. Results indicated the concept should be feasible at the device level. Practicality in a system application can be realized but it will be dependent on the particular circuit implementation used. Consequently, IBM-FSD recommends further investigation of the threshold measurement concept, particularly in the area of E^2PROMS due to their enhanced system applicability.

TABLE OF CONTENTS

SECTION		PAGE
1.0	INTRODUCTION	1
2.0	DEVICE DESCRIPTION AND PRINCIPLES OF THE PROPOSED TEST	2
	2.1 FLOATING GATE PRINCIPLE	2
	2.2 MOSTEK MK2716 DESCRIPTION	4
	2.3 CELL THRESHOLD MEASUREMENT MODE	8
3.0	EXPERIMENTAL APPROACH	11
	3.1 CHARACTERIZATION SAMPLES	11
	3.2 TEST EQUIPMENT	12
	3.3 TYPES OF MEASUREMENTS	14
4.0	TEST RESULTS AND DISCUSSION	15
	4.1 FUNCTIONAL PERFORMANCE	15
	4.2 TEST MODE EVALUATION	17
	4.3 SYSTEM IMPLEMENTATION	26
5.0	CONCLUSIONS AND RECOMMENDATIONS	28
APPENDIX I	MOSTEK MK2716 DATA SHEET	30



LIST OF ILLUSTRATIONS

FIGURE		PAGE
2-1	EPROM STORAGE CELL	2
2-2	THRESHOLD VOLTAGE MARGINS	2
2-3	MK2716 PIN CONFIGURATION	6
2-4	MK2716 BLOCK DIAGRAM	7
2-5	WORD LINE/STORAGE CELL SCHEMATIC	9
3-1	CHARACTERIZATION TIMING	13
4-1	ACCESS TIME VS. TEMPERATURE	16
4-2	SUPPLY CURRENT VS. SUPPLY VOLTAGE	16
4-3	SINGLE CELL PROGRAMMING CHARACTERISTICS	17
4-4	MAXIMUM AND MINIMUM PROGRAMMED THRESHOLDS	18
4-5	NET OF PROGRAMMING AND DEPROGRAMMING	19
4-6	COMPOSITE PROGRAMMING CHARACTERISTICS	20
4-7	THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE	21
4-8	ERASURE CHARACTERISTICS	22
4-9	PROGRAMMING REPRODUCIBILITY	23
4-10	ACCESS TIME VS. VPP	25

1.0 INTRODUCTION

Since its introduction in 1972 the UV EPROM has taken on an important role in the electronics industry. Unfortunately, to date, no conclusive evidence exists on the reliability of data retention in EPROMs in severe environment applications. This has hindered their application in military systems. The inherent need to gather such data over long periods of time adds to the difficulty of acquiring an adequate data base to support military applications. IBM has proposed an alternate approach whereby, given the appropriate on-chip circuitry, the user can periodically monitor the integrity of all programmed and non-programmed cells thus providing a timely indication of marginal data storage so that corrective action can be instituted. This minimizes the need to guarantee long term data retention. A single vendor device was found which had incorporated in it a similar function, but for a different purpose. IBM chose to use this function as a vehicle for evaluating the concept.

The present RADC program provides for an assessment of the utility of this concept to facilitate the use of EPROMs in military equipment.

Summarizing the results of this effort, it has been determined that such a concept is achievable at the device level. Although limitations exist due to the present circuit implementation, practicality at the system level can be realized.

2.0 DEVICE DESCRIPTION

2.1 Floating Gate Principles

The principles of the UV EPROM are best explained by the operation of the floating gate storage cell. The storage cell consists of two polysilicon gates as illustrated below, a conventional control gate, and an electrically isolated floating gate. The floating gate has two stable states, an erased state, and a programmed state. Programming is accomplished by raising both the drain and control gate to a high voltage causing a high electric field. Electrons traveling in the channel are accelerated by the field and some gain enough energy to leave the channel, traverse the oxide, and become trapped on the floating gate. Once trapped on the floating gate they remain there unless erased by exposure to UV light.

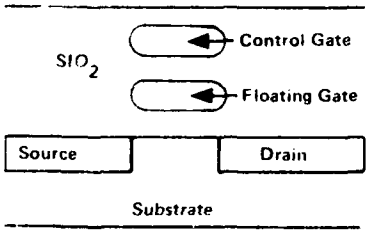


FIGURE 2-1 EPROM STORAGE CELL

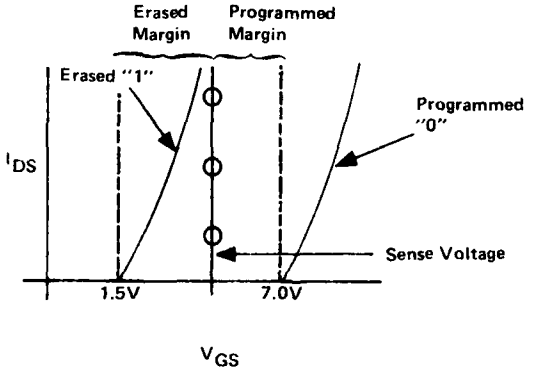


FIGURE 2-2 THRESHOLD VOLTAGE MARGINS

The threshold voltage of a cell properly programmed as a "0" is greater than approximately 7.0V, while that of a properly erased "1" is approximately 1.5V. During a read operation, the control gate is biased to approximately 5.0V (determined by V_{CC} and the read mode program voltage V_{PP}). I_{DS} will flow only for a $V_T < 5.0V$, providing the basis for sensing the cells state. The difference between the programmed (or erased) threshold voltage and the 5.0V sense voltage will be called the programmed (or erased) margin, as illustrated in Figure 2-2.

Under stressing environmental conditions, or if certain fabrication defects exist, some of the stored charge may leak off a programmed gate or may leak onto an erased gate, gradually decreasing the margin of that cell. In standard EPROMs, cells possessing poor data retention characteristics such as this can not be practically identified prior to failure. Other failure modes such as wearout due to many write/erase cycles are also unidentifiable in a standard EPROM without special techniques.

A device implemented with a mode capable of measuring the programmed and erased threshold voltage allows the device margin to be monitored periodically, thereby minimizing the chance of a data retention failure in a critical environment.

2.2 Mostek 2716 Description

The Mostek MK2716 is an ultra-violet erasable electrically programmable read only memory organized 2048 words by 8 bits. It is fabricated using N-channel double poly-silicon silicon gate technology. The MK2716 provides six standard operating modes and two special characterization modes*, as indicated in Table 2-1.

MODE	$\overline{CE}$	VPP	$\overline{OE}$	OUTPUTS
READ	V_{IL}	+5	V_{IL}	DATA OUT
DESELECT	DON'T CARE	+5	V_{IH}	HIGH IMPEDANCE
POWER DOWN	V_{IH}	+5	DON'T CARE	HIGH IMPEDENCE
PROGRAM	PULSED V_{IL} TO V_{IH}	+25	V_{IH}	DATA IN
PROGRAM VERIFY	V_{IL}	+25	V_{IL}	DATA OUT
PROGRAM INHIBIT	V_{IL}	+25	V_{IH}	HIGH IMPEDANCE
*THRESHOLD MEASUREMENT	+25V	VARY OV TO V_T	V_{IL}	DATA OUT
*DEPROGRAM	+25V	PULSED OV TO +25V	V_{IL}	HIGH IMPEDANCE

$\overline{CE}$ - Chip Enable (Active Low)

$\overline{OE}$ - Output Enable (Active Low)

VPP - Programming Supply Voltage

TABLE 2-1 MODE SELECTION

A detailed description of the device, its standard operating modes and the specified timing requirements are included on the attached Mostek data sheet (Appendix I).

The threshold measurement mode provides a limited means to measure the threshold margin of any cell within the array for data retention evaluation. Although Mostek is running high volume production on the MK2716 implemented with the threshold measurement mode, they are also maintaining production of the standard version without the special modes. Since this is an experimental technique, Mostek has chosen not to promote either special mode at this time. This mode will be discussed further in Section 2.3.

The deprogramming mode allows investigation of charge loss effects due to the programming of other cells. While not explicitly relevent to threshold measurement, it does merit discussion for general information. The deprogramming mode was not investigated in this study, although the effects of deprogramming during programming are evident in the data of Section 4.

Deprogramming occurs when charge on a cell's programmed floating gate is lost due to the programming of other cells along the same word line. This occurs when a cell previously programmed to a "0" state (charged floating gate), has its gate raised to 25V by the programming of another cell on the same word line. Due to asperities that exist at the

polysilicon/silicon dioxide interface of the floating gate, some charge may be lost as a result of the high electric field induced by the 25V applied to the gate. Since 16 cells share the same word line, a single cell can see as many as 15 deprogramming cycles, or 750 ms of deprogramming time, assuming a 50 ms programming pulse width.

The purpose of the deprogramming mode is to simultaneously impress upon the floating gate of every storage cell in the array the maximum amount of deprogramming that could possibly be seen by any single cell during programming, thus uniformly deprogramming all cells.

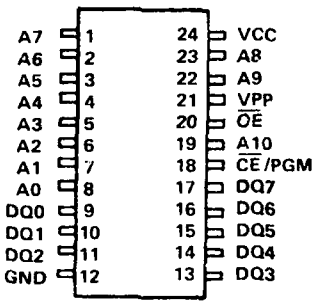


FIGURE 2-3 MK2716 PIN CONFIGURATION

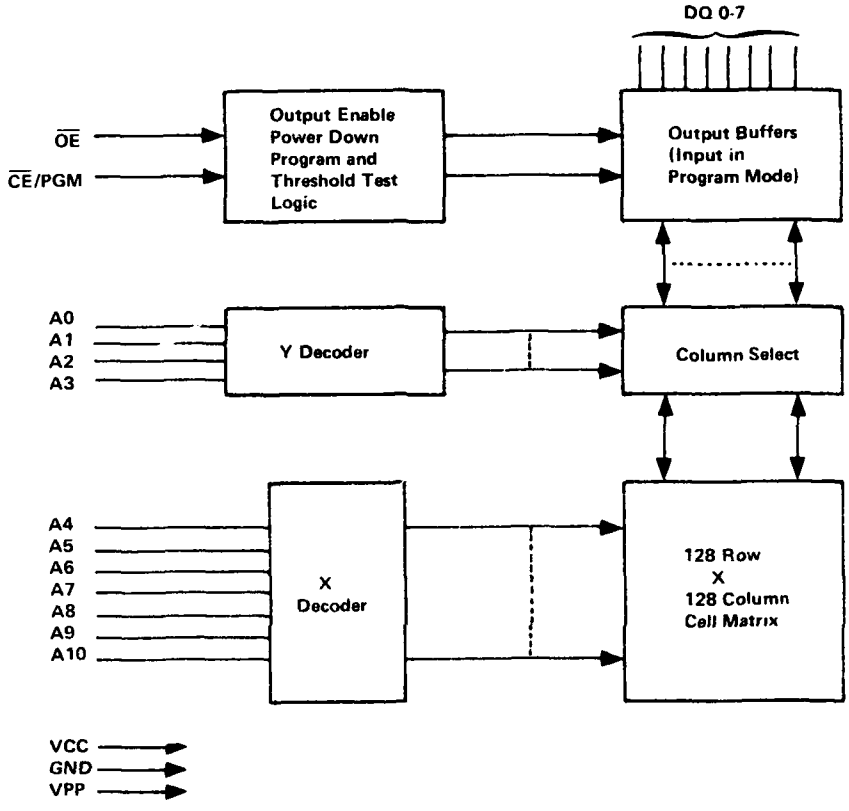
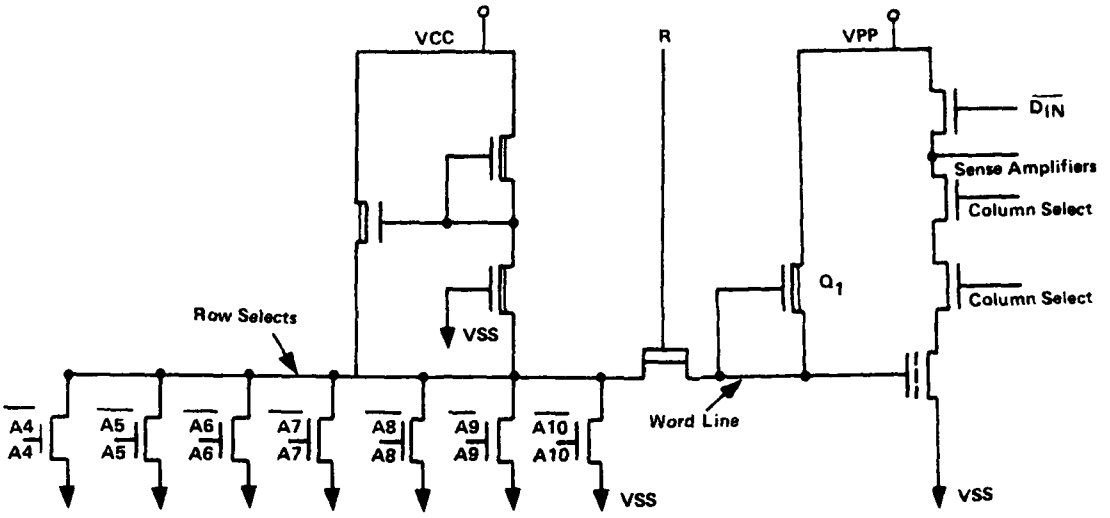


FIGURE 2-3 MOSTEK MK2716 BLOCK DIAGRAM

2.3 Cell Threshold Measurement Mode

The threshold measurement mode provides the user with the capability to vary the gate bias on the storage cell until a change in the output state occurs. The change implies the gate bias just slightly exceeds the V_T of the cell. The VT and the margin in its programmed state. By applying the proper address levels, addressing is accomplished just as it is in any of the standard modes allowing access to any of the 16384 cells in the array. By using this mode it is possible to program a device, evaluate its programmed margin, and periodically monitor the margin to verify it is within predetermined boundaries.

The threshold measurement mode was implemented by adding (to the standard design) a high voltage sense circuit on the $\overline{CE}$ input and associated logic allowing the word line voltage to be controlled by V_{PP} during read mode conditions (when sense amp and output buffers are enabled). Prior to this modification the word line voltage was determined by V_{CC} in all but the program mode. The V_{CC} circuitry was optimized initially to provide faster response at the word line thereby reducing access time to an erased "1" state. Since the threshold measurement mode relys on the slower single depletion device (Q1 in Figure 2-5) tied to the word line and V_{PP} to generate the word line voltage, access time is increased. This phenomena will be discussed further in Section 4. The simplified word line/storage cell schematic illustrates the operation of this mode.



R – Internally generated signal = "0" during Program, Threshold Test & Deprogram modes
"1" during all other modes

$\overline{D_{IN}}$ – Internally generated signal = Inverted Data In during programming mode
"0" during all other modes

FIGURE 2-5 WORD LINE/STORAGE CELL SCHEMATIC

The ability to continuously vary the word line voltage and hence the storage cell gate voltage allows determination of the precise voltage at which the floating gate cell will cause the sense amp to read a "1". This is done simply by increasing V_{PP} in the test mode while monitoring the output of whichever bit is to be measured. When the output switches from a "0" to a "1", the select gate voltage has increased to a level sufficient to overcome the offset due to the floating gate charge allowing I_{DS} to switch the state of the sense amplifier thereby indicating the threshold voltage (V_T) of that cell.

Although the threshold test mode functions well in the 7V to 12V range typical of a programmed cell, the particular circuit used imposes limitations when the programmed threshold voltage value is outside of the 5V to 14V range. These limitations can be attributed to two individual functions, and therefore will be discussed separately.

The limitation on the measurement of very high thresholds is due to the minimum voltage on V_{PP} required to select the deprogramming mode. As indicated in Table 2-1, a 25V pulse on V_{PP} is required for deprogramming. When operating in the threshold test mode, it was found that exceeding a 14V level on V_{PP} caused selection of the deprogramming mode and deselection of the threshold test mode. Therefore, cells which have programmed thresholds greater than this voltage cannot be measured.

The second, more significant limitation, prevents measuring the threshold voltage of a cell less than 5.0V, such as that of an erased cell. Reviewing Figure 2-5, as V_{PP} is decreased to a voltage less than V_{CC}, a small current flow will result through the depletion device in series with the word line, the current increasing as V_{PP} decreases. Since the V_{PP} load device has a significantly smaller aspect ratio than the V_{CC} load circuit or the series FET, a large percentage of the $V_{CC} - V_{PP}$ potential is dropped across the V_{PP} device. Therefore, for $V_{PP} < V_{CC}$ the word line voltage no longer equals that of V_{PP}. In fact, it is not possible to lower the word line voltage to the actual threshold voltage of a fully erased cell (approximately 1.5V). Therefore, accurate

threshold measurements below 5.0V are not possible. Without the ability to measure the margin of an erased cell, failure due to charge accumulation cannot be detected prior to failure.

It must be recognized that the circuitry for the threshold test mode and deprogramming mode was added to an existing design and was therefore not optimized. Had these modes been considered at the initial design of the device the limitations discussed could have been avoided.

3.0 EXPERIMENTAL APPROACH

This section discusses the samples characterized for this study, the test equipment used in performing the characterization, and identification of the types of tests performed.

3.1 Characterization Samples

Thirteen commercial 16K EPROM samples were obtained for this study. They were packaged in hermetically sealed, side brazed, ceramic dual in line packages having three different identification markings.

VENDOR MARKING	QUANTITY	DATE CODE	IBM SAMPLE NO.
Unmarked	4	Unmarked	1-1, 2, 3, 4
MK2716T-7	5	7928	2-1, 2, 3, 4, 5
MK2716T-6	5	7923	3-1, 2, 3, 5

The -6 designation indicates vendor screening to 350NS maximum address access time (t_{AA}) whereas the -7 indicates 390NS maximum t_{AA}.

3.2 Test Equipment

A Siemens/Computest V-200 Semiconductor Memory Test System was the primary characterization tool used for this study. The V-200 is a programmable dedicated memory tester providing address, clock, and data signals to the device under test. Timing edges can be varied during testing. All supply and signal voltage levels may be varied independently. Address generation by microprogram control allows many different sequences to be exercised. Data generation is by algorithm allowing a great variety of data patterns to be used.

A bench set-up consisting of two HP8007B Pulse Generators and two Dual HP power supplies were used for static device testing. An IBM built D.C. tester providing a continuous current vs. voltage plot was used for D.C. parametric characterization.

The V-200 tester was programmed with specification sheet voltages and timing for read mode characterization. For threshold test mode characterization data either nominal timing or extended cycle timing was used. The extended cycle was used to verify the word line had sufficient time to settle to its final value before valid data was to be read. Programming was accomplished using Mostek data sheet timing specifications. For all programming, a maximum 33% programming duty

cycle was used to avoid excessive power dissipation, although this is not specified in the Mostek data sheet.

Figure 3-1 presents the specific timing used for the testing performed in this study.

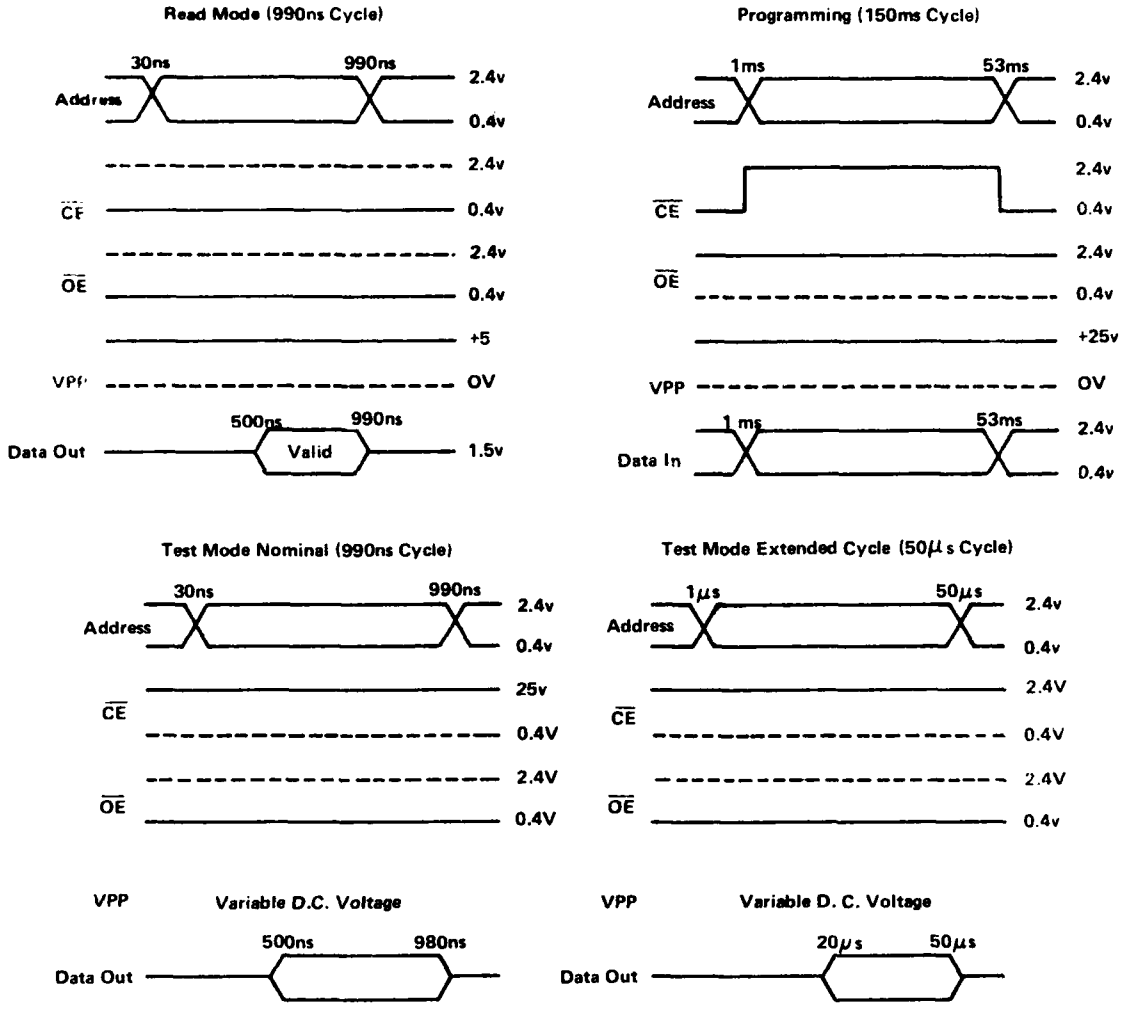


FIGURE 3-1 CHARACTERIZATION TIMING

3.3 Individual Measurements

A variety of parameter dependencies, as listed below, were measured as part of the investigation. Specific results are described in the next section.

Functional Performance:

- Address access time vs. case temperature
- Supply current vs. supply voltage
- Supply current vs. $\overline{CE}$ voltage

Test Mode Evaluation:

- Programming characteristics
- Threshold voltage vs. supply voltage variations
- Erasure characteristics
- Threshold reproducibility
- Threshold voltage vs. time under ambient conditions
- Address access time vs. V_{PP}

4.0 TEST RESULTS AND DISCUSSION

This section presents the actual data taken and discusses conclusions drawn from that data.

4.1 Functional Performance

Three basic tests were performed to verify the devices with the test mode incorporated in them would function as normal production EPROMs over the temperature and voltage ranges to be dealt with in this study.

Address access time as a function of case temperature in read mode is plotted in Figure 4-1. This data was taken on sample #1-2 at V_{CC} = 5.00V only. Access time varied considerably over the MIL temperature range with a worst case of 588NS at +125°C. The device did function without error over this range from a supply voltage of 4.75V to 5.25V although this is not plotted. The change in the slope of this curve at 100°C is considered insignificant since it was not observed on other samples.

Supply current as a function of supply voltage in read mode is plotted in Figure 4-2. The negative current derives from the influence of V_{pp} which was 5.0V during this test. Read mode and standby current measurements were taken at room temperature.

Supply current as a function of $\overline{CE}$ voltage was measured to determine the $\overline{CE}$ input threshold at which the device switches from the power down mode to the threshold test/deprogramming modes. Data taken but not presented indicates this selection occurs in the 13V to 15V range varying among devices. The $\overline{CE}$ voltage used for selection of the threshold test/deprogramming mode in this study is 25V.

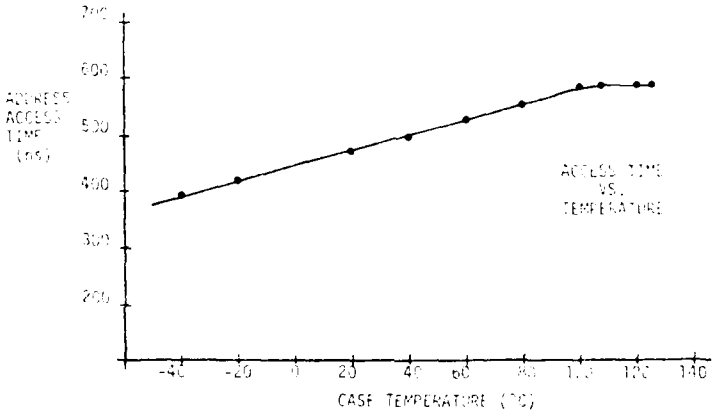


FIGURE 4-1 ACCESS TIME VS. TEMPERATURE

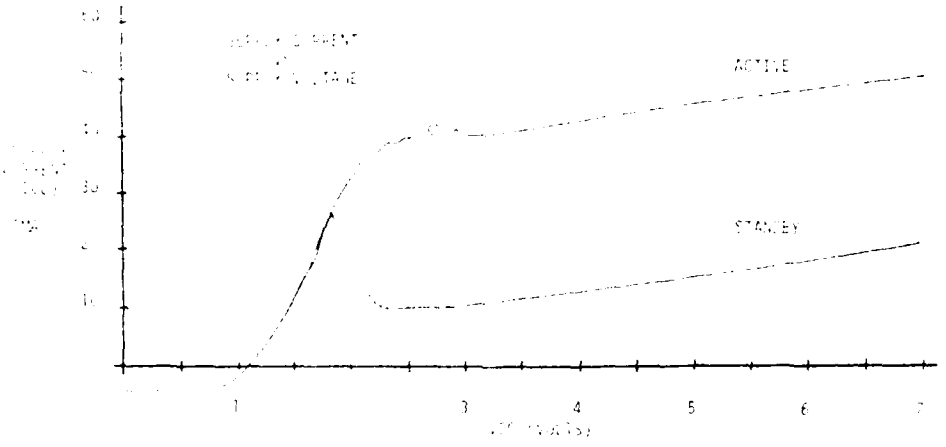


FIGURE 4-2 SUPPLY CURRENT VS. SUPPLY VOLTAGE

4.2 Test Mode Evaluation

This section discusses testing performed to investigate the utility of the test mode and its dependence on measurement conditions. Because of the limitations on threshold measurements imposed by the present MK2716 circuit implementation, no threshold data is presented outside the 5.0V to 14.0V range.

Programming Characteristics

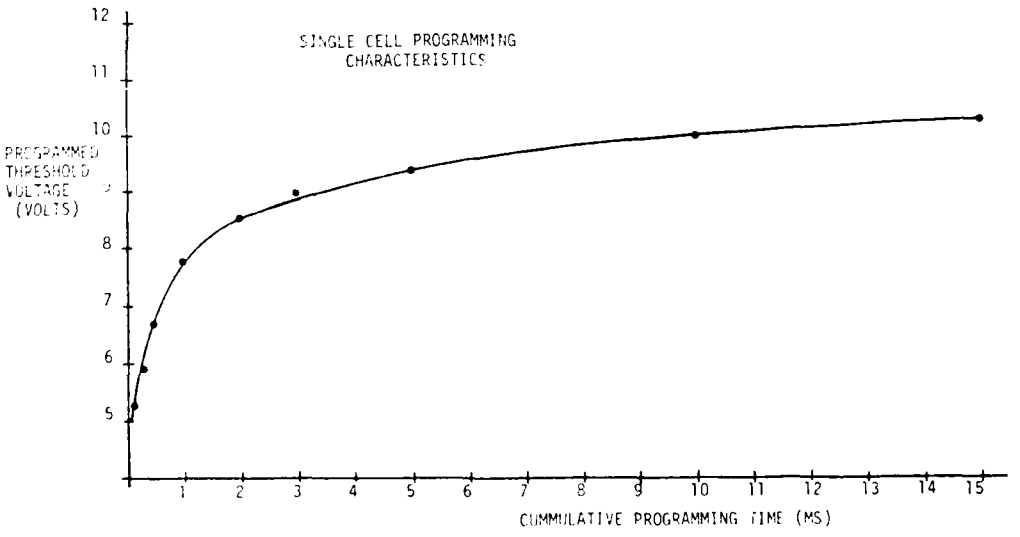


FIGURE 4-3 SINGLE CELL PROGRAMMING CHARACTERISTICS

Threshold voltage as a function of total programming time (accumulated pulse widths) was analyzed to evaluate the programming profile of an individual cell and that of an entire array. Figure 4-3 shows the storage cell threshold voltage as a function of cummulative programming time (i.e. no erasure between steps). A single word was selected and bit 0 in that word characterized. During programming only that single location was programmed, eliminating any effects of deprogramming. Threshold measurements for this case were taken with static conditions on the device. As the figure shows, at 1.8ms, 66% of the resultant V_T is reached and 90% is reached at 15ms programming time. This demonstrates that the vendor's specified program pulse width of 50ms insures with good margin that most of the V_T shift possible by programming will be realized. (As will be described however, deprogramming becomes a factor at this pulse width.)

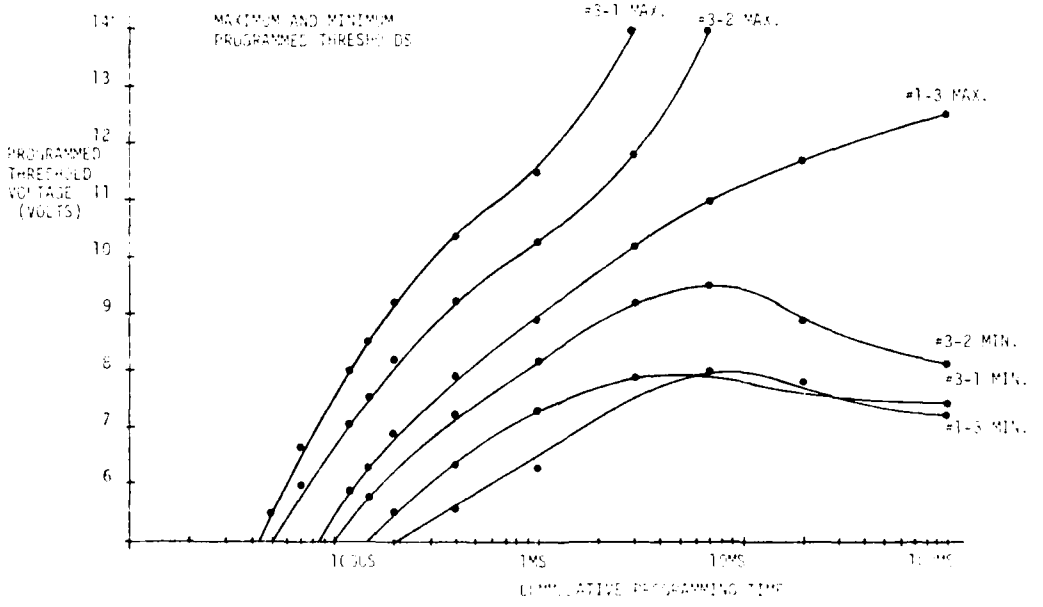


FIGURE 4-4 MAXIMUM AND MINIMUM PROGRAMMED THRESHOLDS

Figure 4-4 portrays the significance of deprogramming. This figure shows for three devices the highest and lowest programmed thresholds in each array as a function of cumulative programming time. Since only the extreme threshold voltages of the array were measured at each programming increment, considerable variations exist from the curve for an individual cell, particularly since the cell locations yielding minimum and maximum thresholds also change. The curves for minimum threshold voltage reveal the significant effect of deprogramming. The curve shape derives from the sum of two individual functions. (Figure 4-5)

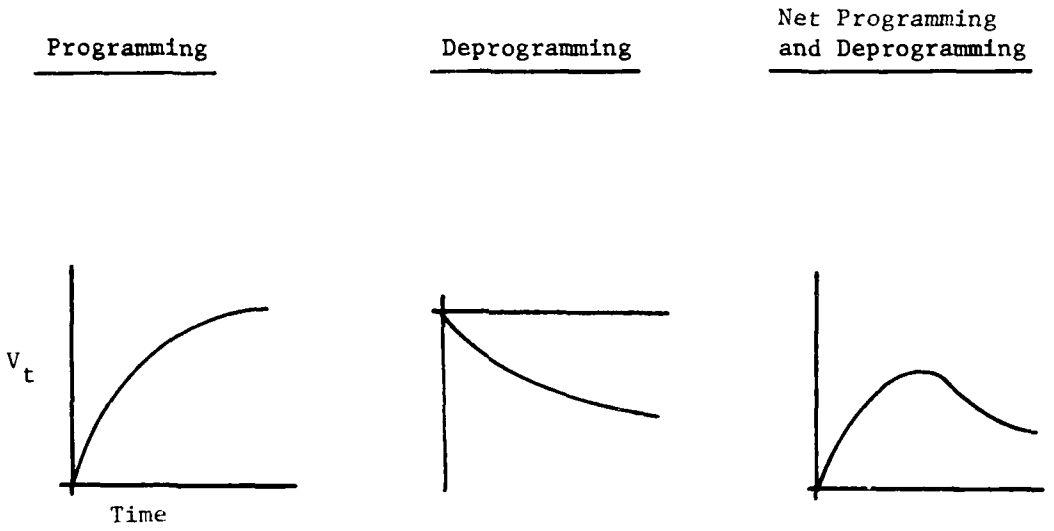


FIGURE 4-5 NET OF PROGRAMMING AND DEPROGRAMMING

To maximize the minimum threshold voltages within the array, a 10ms programming pulse width would be optimum based on the sample evaluated.

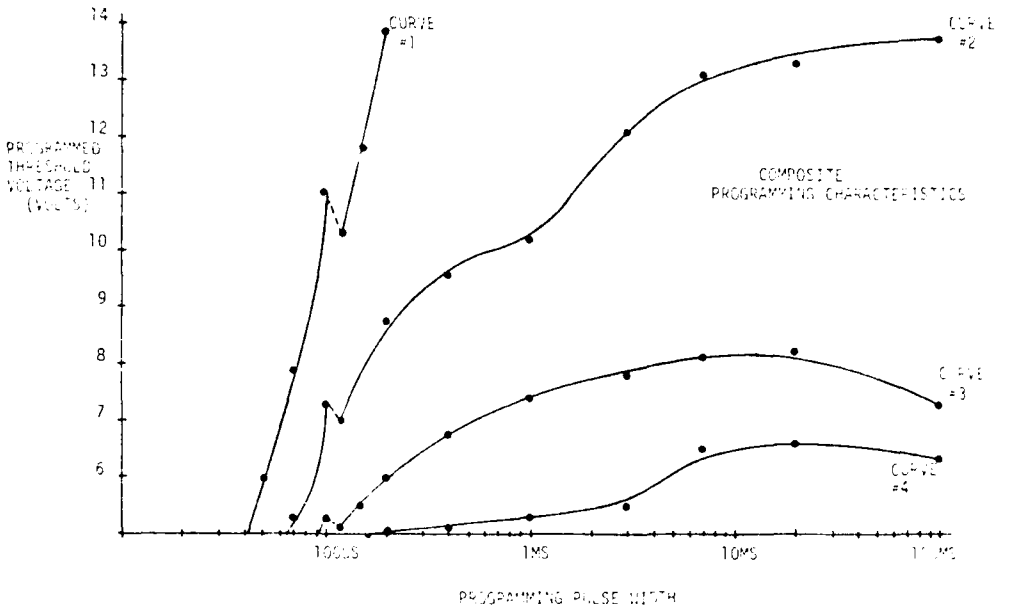


FIGURE 4-6 COMPOSITE PROGRAMMING CHARACTERISTICS

Figure 4-6 summarizes the best and worst case programmed margins for twelve devices. The four curves are:

#1 Largest programmed threshold voltage for any cell of any sample.

#2 Average of the largest programmed threshold voltage of each of the 12 samples.

#3 Average of the smallest programmed threshold voltage of each of the 12 samples.

#4 Smallest programmed threshold voltage for any cell of any sample.

In each case all devices were erased for 15 minutes, programmed with the indicated programming pulse width and measured in the test mode. Only the maximum and minimum programmed threshold voltages for each device were recorded.

Curves #1 and #4 indicate the wide range of possible programmed thresholds within the sample set. Curve #4 indicates the small margin in some cells at any programming pulse width, emphasizing the need for testability as promoted in this study. Curve #3 shows the majority of devices do not exhibit such marginal thresholds indicating devices with larger margins are yieldable. Prior to the implementation of this test mode, the user had little knowledge of how marginal the programmed cells were in the device he was using. This technique allows a user, at any elapsed time of his application, to determine the remaining margin for each cell, providing a timely indication of any potential data retention failure.

Threshold Voltage vs. Supply Voltage Variations

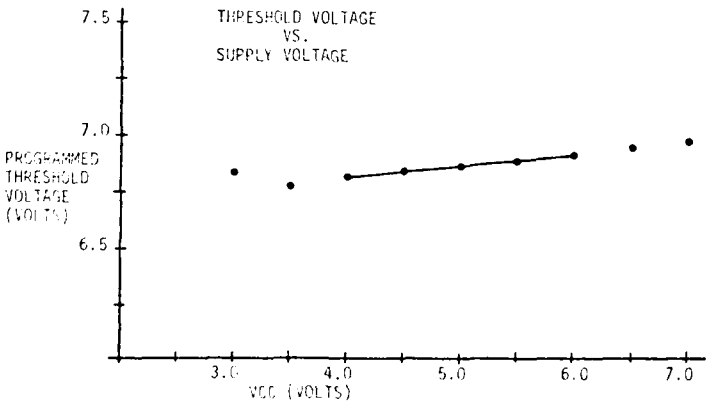


FIGURE 4-7 THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE

Measured threshold voltage as a function of V_{CC} supply voltage was investigated to determine the test mode sensitivity to supply variations. The minimum programmed threshold location is plotted in Figure 4-7. A $\Delta V_T/\Delta V_{CC}$ = 0.05V/V linear slope was observed over the 4.0V to 6.0V V_{CC} range. This correlates to a 25 MV ΔV_T over the 4.75V to 5.25V V_{CC} operating range. This small change is expected and is not a significant factor in the use of the test mode.

Erasure Characteristics

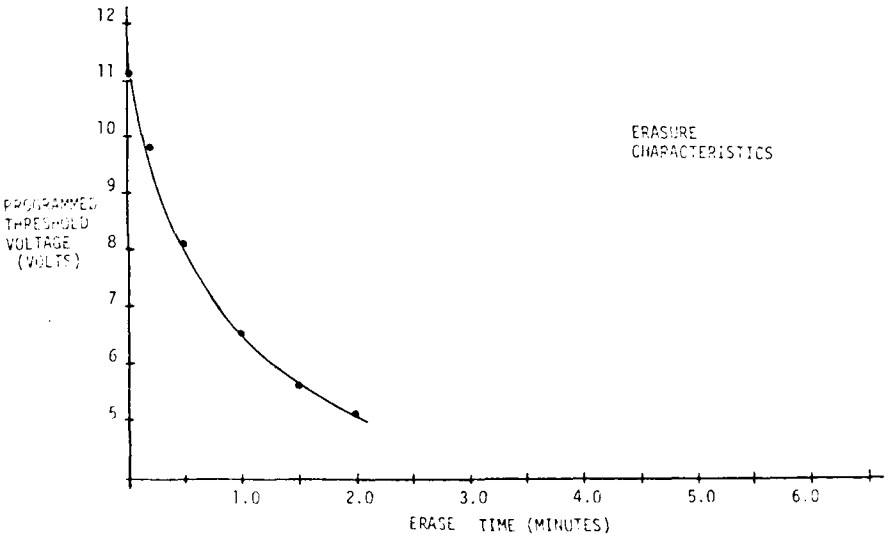


FIGURE 4-8 ERASURE CHARACTERISTICS

UV light erasure characteristics were measured to verify the adequacy of the guard band in the 15 minute vendor specified erase cycle. Testing was performed under the same conditions as the static V_T vs. programming time test earlier in this section. The data, illustrated

in Figure 4-8, was also cumulative having no reprogramming between erasure steps. Due to the limitations on measuring V_T < 5.0V data was not available for values less than this. However, data at the 2 minute interval indicates the threshold voltage has already decreased from 11.1V to 5.0V indicating a large enough rate of change to suggest 15 minutes is adequate for proper erasure.

Threshold Reproducibility

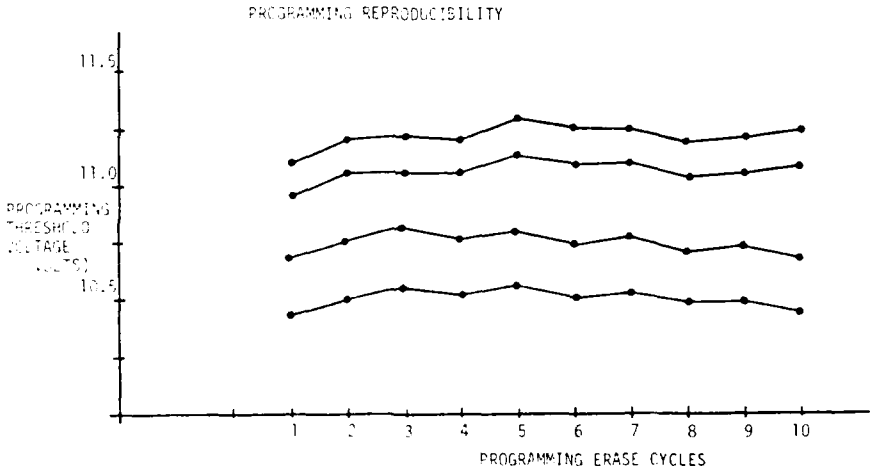


FIGURE 4-9 PROGRAMMING REPRODUCIBILITY

To establish the reproducibility of the programming/measurement operation, four individual cells in two samples were erased, programmed, and characterized in the test mode for a total of ten cycles. For this test, temperature, V_{CC}, V_{PP}, t_{PW}, and t_{ERASE}, were held constant

at nominal values. Since repeated V_T measurements reproduced closely, the small variations observed in Figure 4-9 were apparently dominated by programming irreproducibility. The fact that for each step, the V_Ts of all cells change in the same direction implies variations are not within the device but are caused by minor fluctuations in the test apparatus. This test was not intended to investigate write-erase cycle wearout mechanisms which are known not to occur for such a limited number of cycles.

Threshold Voltage vs. Time Under Ambient Conditions

Threshold voltage shift due to ambient light exposure was investigated for short periods of time to determine if special precautions were needed to maintain a controlled experiment. Data taken on the minimum and maximum threshold locations, and seven random locations on a single sample for seven intervals over 55 hrs. indicated negligible change. For this reason, devices which were to be characterized in the threshold test mode for no longer than 24 hours after programming were not covered with the protective opaque tape used otherwise. This test also demonstrated the negligible effects of any other uncontrolled factors in the normal lab environment.

Address Access Time vs. V_{PP}

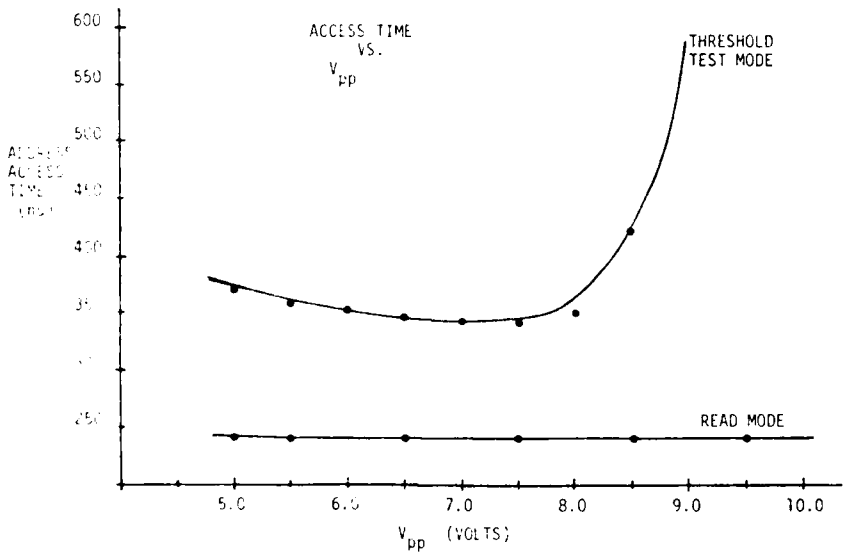


FIGURE 4-10 ACCESS TIME VS. V_{PP}

The address access time will be slower in the test mode than in the read mode. This is because the threshold test mode uses a single depletion device tied to V_{PP} to drive the word line rather than the high speed circuitry connected to V_{CC} in the read mode.

Testing was performed to characterize and compare t_{AA} in both modes. Data presented in Figure 4-10 shows this comparison as a function of total programming time. At $V_{PP} = V_{CC} = 5.0V$, access time is 120ns slower in the test mode than in the read mode for a 50ms t_{PW}. Further data taken but not shown identified sample #1-4 as being the worst case device exhibiting a τ_{AA} difference of 190ns at 5.0V. This difference could be significant in some system applications since the timing might have to be modified for test mode addressing.

4.3 System Implementation

Implementation of the threshold test mode can be accomplished in a variety of ways. This section discusses one possible system application.

Configuring the system to independently utilize the threshold test mode as a "self-check" would be an optimum application. The specific steps comprising this application are:

1) Load system RAM with the contents of the EPROM (assumes data is valid) or load system RAM with known valid data on diagnostic tape.
2) Apply required test mode select signals to EPROM vendor test.
3) Raise V_{PP} to the margin selected for programmed "0"s.
4) Compare EPROM data to known valid data in RAM and check for errors.
5) Lower V_{PP} to the margin selected for erased "1"s.
6) Compare EPROM data to known valid data in RAM and check for errors.

Any comparison errors indicate inadequate margin and the need for corrective action. A failing "0" may be reprogrammed individually. A failing "1" requires complete U.V. erasure of the entire device (provided the failure is indicative of charge accumulation on a cell rather than charge trapping in the oxide). This demonstrates the real

power of this technique will be realized in electrically erasable devices. The E^2PROM offers the advantage of a practical in system erase which could be performed by the system when detecting an inadequate "1".

5.0 CONCLUSIONS AND RECOMMENDATIONS

The results of this effort have provided evidence of the feasibility of a measurement concept to assess the retention margin of an EPROM storage cell, and the practicality of implementing this concept in production hardware.

While the particular circuitry incorporated by Mostek for other purposes proved useful in evaluating the proposed concept, cell threshold measurement was limited to the programmed "0" state only, making this device inadequate for margin test applications.

Results of data taken on the device in its operable range provided evidence of the practicality of system level integration. Measured data demonstrated insensitivity to supply variations and minimal test mode address access time degradation. No significant limiting factors were encountered during the study (although more detailed investigation is necessary to confirm this) indicating conceivable system level applicability. The wide spread of programmed threshold voltages exhibited some marginally programmed cells emphasizing the need to develop such a test technique. The significant effect deprogramming had on decreasing the cell margin of programmed cells was observed and from this data an optimum programming pulse width was determined for the samples evaluated.

From the positive results obtained in this study, the implementation of such test in EPROM devices encourages applications such as system self-testability, vendor production characterization, and prescreening by critical users.

While no vendors have revealed their plans, there are indications that some vendors are considering test mode implementation in their forthcoming EPROMs and E^2PROMs.

Ultimately, the most favorable application of this technique would be in electrically erasable PROMs. Integrated into the system, the E^2PROM could be reprogrammed and reerased contingent upon inadequate margin measurements. This type of non-automatic refresh would provide a device with more dependable data retention while minimizing write/erase cycle wearout concerns. Consequently, IBM-FSD recommends further investigation of the threshold test mode particularly in the area of E^2PROMs.

APPENDIX I

MOSTEK MK2716 DATA SHEET

MOSTEK

2048 x 8-BIT PROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (T)-5/6/7/8

FEATURES

- Replacement for popular 2048 x 8 bit 2716 type EPROM
- Single +5 volt power supply during READ operation
- Fast Access Time in READ mode

P/N	Access Time
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

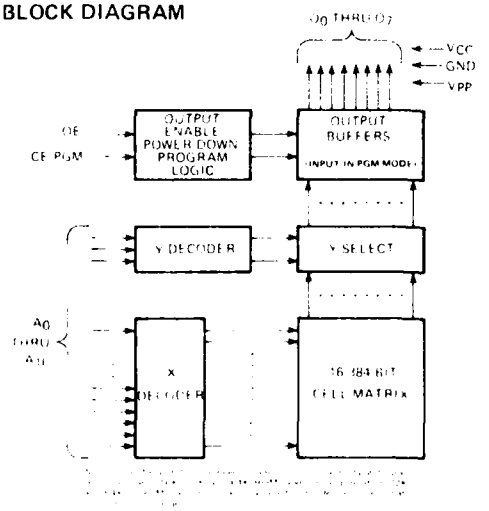
- Low Power Dissipation: 525 mW max active
- Power Down mode: 132 mW max standby
- Three State Output OR-tie capability
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50 msec pulse
- Pin Compatible with Mostek's Wide Word Memory Family
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid

DESCRIPTION

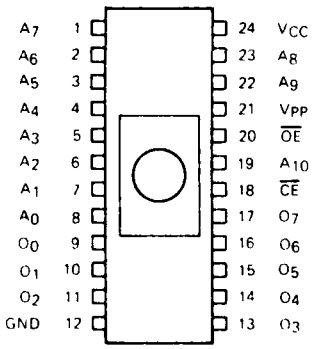
The MK2716 is a 2048 x 8 bit electrically programmable ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525 mW maximum active power to 132 mW maximum for an overall savings of 75%

BLOCK DIAGRAM



PIN OUT



A0 A10 ADDRESSES
CE/PGM CHIP ENABLE PROGRAM
OE OUTPUT ENABLE
O0 O7 OUTPUTS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS (Except VPP) ..... -0.3V to +6V
Voltage on VPP supply pin relative to VSS ..... -0.3V to +28V
Operating Temperature TA (Ambient) ..... $0°C \leq TA \leq 70°C$
Storage Temperature (Ambient) ..... $-55°C \leq TA \leq +125°C$
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED D.C. OPERATING CONDITIONS AND CHARACTERISTICS[1,2,4,8]

($0°C \leq TA \leq 70°C$) ($VCC = +5V \pm 5\%$, $VPP = VCC$)[3]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		Vcc+1	Volts	
V_{IL}	Input Low Voltage	-0.1		0.8	Volts	
I_{CC1}	VCC Standby Power Supply Current ($\overline{OE}$ = VIL, $\overline{CE}$ = VIH)		10	25	mA	2
I_{CC2}	VCC Active Power Supply Current ($\overline{OE}$ = $\overline{CE}$ = VIL)		57	100	mA	2
I_{PP}	VPP Current (VPP = 5.25V)			6	mA	2,3
V_{OH}	Output High Voltage (IOH = -400 μA)	2.4			Volts	
V_{OL}	Output Low Voltage (IOL = 2.1mA)			.45	Volts	
I_{LI}	Input Leakage Current (VIN = 5.25V)			10	μA	
I_{LO}	Output Leakage Current (VOUT = 5.25V)			10	μA	

AC CHARACTERISTICS[1,2,5]

($0°C \leq TA \leq 70°C$) ($VCC = +5V \pm 5\%$, $VPP = VCC$)[3]

		-5		-6		-7		-8			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{AVQV}	Address to Output Delay ($\overline{CE}$ = $\overline{OE}$ = VIL)		300		350		390		450	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay ($\overline{OE}$ = VIL)		300		350		390		450	ns	6
t_{GLQV}	Output Enable to Output Delay ($\overline{CE}$ = VIL)		120		120		120		120	ns	10
t_{EHQZ}	Chip Deselect to Output Float ($\overline{CE}$ = VIL)	0	100	0	100	0	100	0	100	ns	9
t_{AXQX}	Address to Output Hold ($\overline{CE}$ = $\overline{OE}$ = VIL)	0		0		0		0		ns	

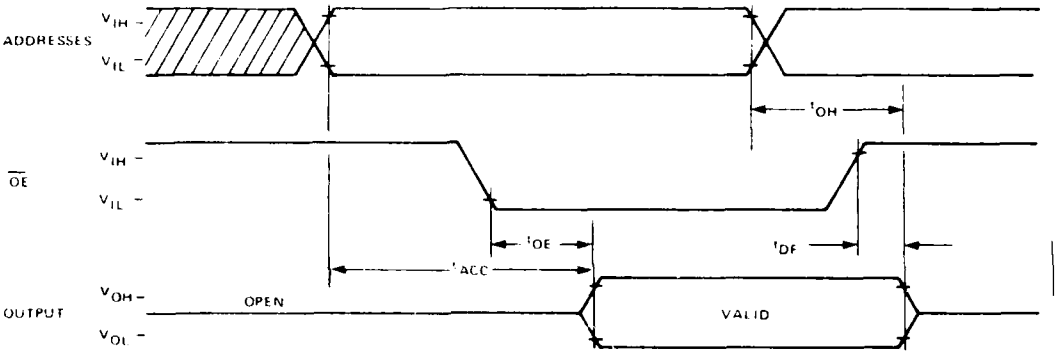
CAPACITANCE
(TA = 25°C)[8]

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	7
C_{OUT}	Output Capacitance	8	12	pF	7

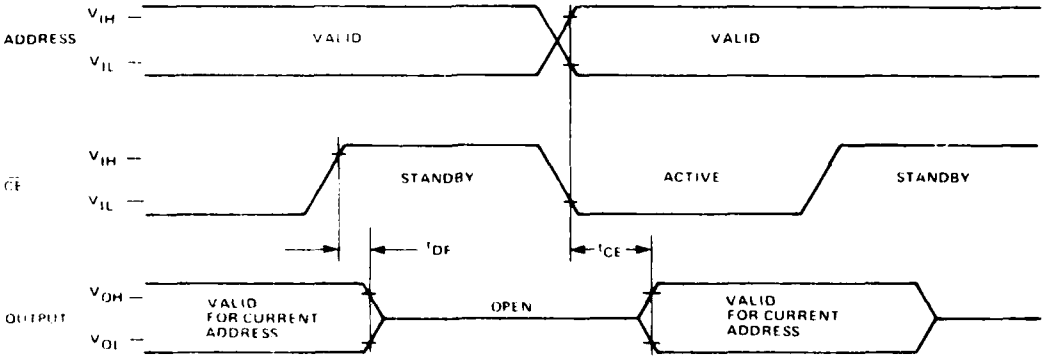
NOTES

1. VCC must be applied on or before VPP and Removed after or at the same times as VPP
2. VPP and VCC may be connected together except during programming In which case the supply current is the sum of ICC and IPP1
3. The tolerance on VPP is to allow use of a driver circuit to switch VPP from VCC to +25V in the READ and PROGRAM mode respectively
4. All voltages with respect to VSS
5. Load conditions 1TTL load and 100pF tr tf 20ns reference levels are 1V or 2V for inputs and 8V and 2V for outputs
6. tOE is referenced to $\overline{CE}$ or the addresses whichever occurs last
7. Effective Capacitance calculated from the equation C V where V 3V
8. Typical numbers are for TA 25 C and VCC 5 0V
9. tDF is applicable to both $\overline{CE}$ and $\overline{OE}$ whichever occurs first
10. OE may follow up to tACC tOE after the falling edge of $\overline{CE}$ without effecting tACC

TIMING DIAGRAMS
READ CYCLE ($\overline{CE}$ = V_{IL})



STANDBY POWER DOWN MODE ($\overline{OE}$ = V_{IL})



PROGRAM OPERATION[8]

D.C. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[1,2]

(TA 25°C ± 5 C) (VCC 5V ±5%, VPP 25V ±1V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
IIL	Input Leakage Current		10	μA	3
VIL	Input Low Level	-0.1	0.8	Volts	
VIH	Input High Level	2.0	VCC + 1	Volts	
ICC	VCC Power Supply Current		100	mA	
IPP1	VPP Supply Current		5	mA	4
IPP2	VPP Supply Current during Programming Pulse		30	mA	5

A.C. CHARACTERISTICS AND OPERATING CONDITIONS[1,2,6,7]

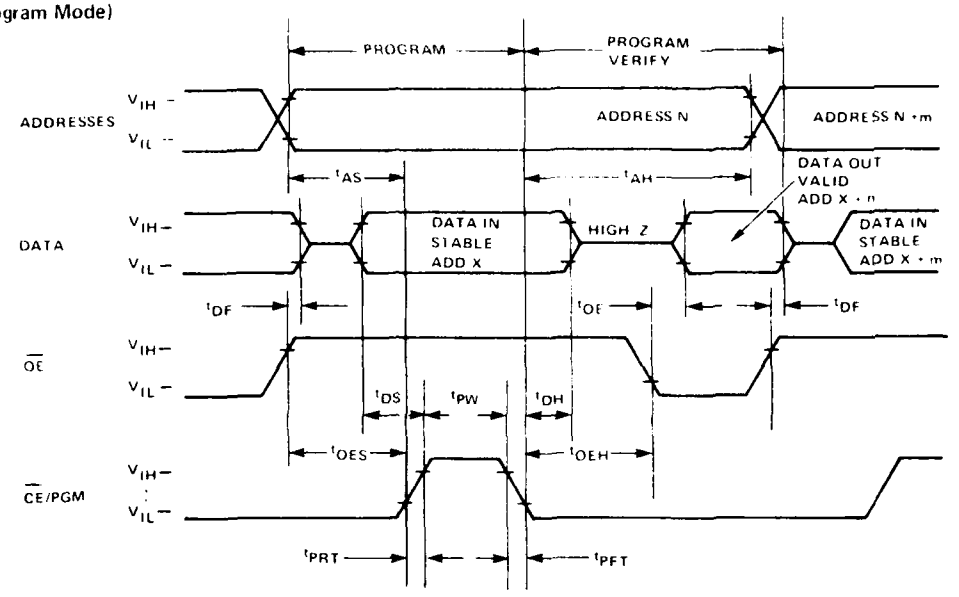
(TA 25 C ± 5°C) (VCC 5V ± 5%, VPP 25V ± 1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
tAS	Address Setup Time	2			μs	
tOES	$\overline{OE}$ Setup Time	2			μs	
tDS	Data Setup Time	2			μs	
tAH	Address Hold Time	2			μs	
tOEH	$\overline{OE}$ Hold Time	2			μs	
tDH	Data Hold Time	2			μs	
tDF	Output Enable to Output Float	0		120	ns	4
tOE	Output Enable to Output Delay			120	ns	4
tPW	Program Pulse Width	45	50	55	ms	
tPRT	Program Pulse Rise Time	5			ns	
tPFT	Program Pulse Fall Time	5			ns	

NOTES

1. [illegible] must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with VPP at 25V.
2. Care must be taken to prevent overshoot of the VPP supply when switching to 25V.
3. [illegible] 45V [illegible] VIN [illegible] 5.25V
4. [illegible] PGM [illegible]
5. [illegible] PGM [illegible]
6. [illegible] 20nsec
7. [illegible] used as timing reference levels.
8. [illegible]

TIMING DIAGRAM
(Program Mode)



MODE SELECTION

MODE	PIN	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	VPP (21)	OUTPUTS
READ		VIL	VIL	+5	Valid Out
STANDBY		VIH	Don't Care	+5	Open
PROGRAM		Pulsed VIL to VIH	VIH	+25	Input
PROGRAM VERIFY		VIL	VIL	+25	Valid Out
PROGRAM INHIBIT		VIL	VIH	+25	Open

VCC(24) = 5V all modes

DESCRIPTION CONTINUED

Programming can be done with a single TTL level pulse, and may be done on any individual location either sequencially or at random. The three-state output controlled by the $\overline{OE}$ input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with Mostek's new 5 volt only microprocessors such as the MK3880 (Z80). The MK2716 is packaged in the industry standard 24-pin dual in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentatin are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MK2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data program is fixed and the intention is to produce large numbers of systems, Mostek also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to MOSTEK, from which the ROM with the desired pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card deck, etc.

READ OPERATION

The MK2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes including READ and STANDBY. A READ operation is accomplished by maintaining pin 18 ($\overline{CE}$) at VIL and pin 21 (VPP) at +5 volts. If $\overline{OE}$ (pin 20) is held active low after addressing (A0 - A10) have stabilized then valid output data will appear on the output pins at access time tACC (address access). In this mode, access time may be referenced to $\overline{OE}$ (tOE) depending on when $\overline{OE}$ occurs (see timing diagrams).

POWER DOWN operation is accomplished by taking pin 18 ($\overline{CE}$) to a TTL high level (VIH). The power is reduced by 75% from 525mW maximum to 132mW. In power down VPP must be at +5 volts and the outputs will be open circuit regardless of the condition of $\overline{OE}$. Access time from a high to low transition of $\overline{CE}$ (tCE) is the same as from addresses (tACC). (See STANDBY Timing Diagram)

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from Mostek will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining VPP at +25V, and $\overline{OE}$ at VIH. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the VCC supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the $\overline{CE}$/PGM pin once addresses and data are stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manor. The program pulse has a minimum width of 45 msec and a maximum of 55msec, and must not be programmed with a high level D.C. signal applied to the $\overline{CE}$/PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain $\overline{OE}$ at VIH, VPP at +25, allow addresses and data to stabilize and pulse the $\overline{CE}$/PGM pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with $\overline{CE}$/PGM at VIL will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce VPP from +25V to +5V. VPP should only be used in the PROGRAM/PROGRAM INHIBIT and PROGRAM VERIFY modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm² is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing a ultra-violet lamp with a 12000μW/cm² power rating. The lamp should be used without short wave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.